SoCWire: a SpaceWire inspired fault tolerant Network on Chip approach for reconfigurable System-on-Chip in Space applications

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Outline

• Data Processing Units based on Xilinx Virtex FPGA
• Future space missions
• Advantage: in-flight and dynamic reconfigurability
• Reconfigurability in space: requirements
• Bus structure based dynamic reconfigurable SoC
• Network-on-Chip approach: SoCWire
• Dynamic reconfigurable architecture
Data Processing Units (DPUs) in space

Data Processing Unit:
• are used as interface between spacecraft and several instrument sensor electronics or heads, providing the operational control and specific data processing of scientific space instruments.

Venus Monitoring Camera (VMC)
- Based on Xilinx Virtex SRAM-cell FPGA
- LEON-2 VHDL model 20 MIPS
- Data rate 14Mbps
- Image processing (compression) in software
• High availability
• Very flexible
• reconfigurability have been used only during the development phase on ground.

Xilinx Virtex FPGAs
• Support dynamic partial reconfiguration
Future Space Missions

PHI on Solar Orbiter (ESA)
- 4Mpixel detector
- data rate up to 500 Mbps

LEVIS
proposed by IDA for Lunar Exploration Orbiter (LEO)
- 5Mpixel detector
- Image acquisition and 1080p HDTV Video (30 Frames/s)
- data rate up to 750 Mbps
Future Space Missions

- Data rate to S/C 20..60 kbps
- Future Space mission demand high-performance on-board processing
- Classical ground processing steps like measurement data inversion and subsequent data evaluation need to be performed on-board
Adaptable on-board processing

VMC CCD anomaly

- Requirement by the scientists: On-board processing must be adaptable to mission specific requirements
Advantage: In-flight and Dynamic reconfigurability
Advantage: In-flight and Dynamic reconfigurability

- Update of processing modules
- **Improvement: maintenance and functionality**
- Especially valuable for space applications with non-accessibility of maintenance points
Advantage: In-flight and Dynamic reconfigurability

- Dynamic partial reconfiguration of modules
  - *run-time adaptive functionality*
  - *reduces resource utilization and power consumption*
Requirements for in-flight reconfigurability and dynamic reconfiguration

• On ground achieved qualification of the system has to be guaranteed even after a module update
  - Effects during dynamic partial reconfiguration have to be considered to prevent an operational interruption of the system
  - Radiation induced errors (SEU “bit-flip”) have to be considered

• **Isolate reconfigurable modules from host system!**
Bus structure based dynamic reconf. SoC

- Static Area → remains unchanged and stores all critical interfaces (CPU, to S/C)
- Partial Reconfigurable Areas (PR-Area) → can be updated during flight
  + Only the updated Module has to be qualified in a delta-qualification step

Xilinx
Virtex-4
FPGA
Bus structure based dynamic reconf. SoC

- Communication between static and PR-areas requires fixed routing
- Xilinx Bus-Macros suitable for bus standards (AMBA, Wishbone)

Host System

Static Area

User Logic

Xilinx Virtex-4 FPGA

Network-on-Chip round table
ESA/ESTEC 2009
“Glitchless” dynamic reconfiguration

- Both modules in reset state:
  - PRM A output “0”
  - PRM B output “1”
Xilinx dynamic reconfiguration behaviour

• Dynamic partial reconfiguration process does not have an explicit activation!
  - New “bits” become active as they are written
• Unpredictable behaviour on the bus!
The architecture model for DPU designs is usually a macro-pipeline system with pre- and post-processing steps in a dedicated structure.
Bus structure based dynamic reconf. SoC

Limitation of bus structure:
- DPU macro-pipeline → Multi master, requires efficient bus arbitration
- SEU in PRM or dynamic reconfiguration process could block bus → stop system
- Failure tolerant bus structure (high efforts) necessary to guarantee data integrity
- No hot-plug ability

Network-on-Chip round table
ESA/ESTEC 2009
Communication Architecture:

- Reconfigurable point-to-point communication
- Support of adaptive macro-pipeline
- High-speed data rate
- Hot-Plug ability to support dynamic reconfigurable modules
- Easy implementation with standard Xilinx Bus-Macros
- Logically separate PRMs from Host System

Network-on-Chip approach
System-on-Chip Wire (SoCWire)
Spacewire

- Established standard in Space applications
- Serial interface
- Layered protocol
- Point-to-point links
- Bi-directional (full-duplex)
- Exchange Level Protocol
  + Link initialization
  + Flow control
  + Detection of link errors
  + Link error recovery
  + Low resource utilization
- Meets all requirements for a fault tolerant NoC
Spacewire

- SpaceWire uses Data-Strobe (DS) encoding
- Performance depends on:
  - Skew-Jitter
  - Technology
SpaceWire character level protocol

Data Characters

Control Characters

Control Characters

FCT Flow Control Token

EOP Normal End of Packet

EEP Exceptional End of Packet

ESP Escape

Control Code

NULL=ESC+FCT

Time Code (ESC+N-Char)

Time

Network-on-Chip round table
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SpaceWire character level protocol

Data Characters

Control Characters

Control Characters

Data Character: 10 Bit
Control Character: 3 Bit
Control Code: 6 Bit
Time Code: 14 Bit

Maximum character length in SpaceWire standard without Time code = 10 Bit

Null=ESC+FCT

Network-on-Chip round table
ESA/ESTEC 2009
SoCWire CODEC

- SpaceWire uses Data-Strobe (DS) encoding
- Performance depends on:
  - Skew-Jitter
  - Technology
- On-chip environment → modified interface
  - 10 Bit parallel data transfer
  - Spacewire standard still supported without time code
  - Scalable data word width (8-128bit)
SoCWire CODEC Performance

Data rates @ 200 MHz

Synthesis report
(Xilinx Virtex-4 LX60 -10)
SoCWire Switch

- SoCWire Switch
  - Scalable data word width (8-128bit)
  - 2 to 32 ports
  - Direct port addressing and header deletion
  - Wormhole Routing
- Entrance
  - Entrance Modules = number of Ports
  - Determines destination port
  - Header deletion
- Matrix
  - Cargo management
  - Connects the individual ports
- Cell
  - Each cell represents connection between 2 ports
  - 4 Ports = 16 Cells
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<table>
<thead>
<tr>
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<th>Max. ( f_{\text{Core}} ) (MHz)</th>
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</tbody>
</table>

- SoCWire Switch 4 Ports synthesis report (Xilinx Virtex-4 LX60-10)

- Maximum data rate equivalent to SoCWire CODEC
Test and Results

- Dynamic reconfigurable macro-pipeline system
- Static area:
  - SoCWire Switch
  - Host System
- Partial reconfigurable Areas
  - PRM 1, 2, 3
- PRMs: configurable packet forwarding Module
- 8 Bit data word width
Test and Results

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Test and Results

- Xilinx Virtex-4 LX60-10
  - Easy implementation with Xilinx standard Bus-Macros
  - Static area distributed over FPGA
- Clock 100 MHz:
  - Data rate macro-pipeline
  - Unidirectional 800 Mbps
  - Bi-directional 700 Mbps
- Dynamically reconfigured one PRM
  - During reconfiguration process communication interrupted
  - After reconfiguration, communication build up automatically without any external action
Test and Results

- FPGA to FPGA communication
- SoCWire CODEC: 8 bit data word width @ 100 MHz → 700 Mbps (Bi-direct.)
SoCWire

• SoCWire
  - Flexible high-speed communication architecture
  - Support of adaptive macro-pipeline
  - Hot-plug ability
  - Suitable for dynamic reconfigurable systems

• SoCWire is distributed under an Open Source license

www.socwire.org
Dynamic Reconfigurable Architecture

- GRLIB LEON-3 from Aeroflex Gaisler
- SoCWire with DMA capability on AMBA
- ICAP Module to access configuration memory
- 3 individual PRMs
Dynamic Reconfigurable Architecture

- SoCWire will be distributed within the GRLIB library of Aeroflex Gaisler
Conclusion

• Configurable SoC proven solution for scientific space applications
• Future space mission demand high performance on-board processing
• In-flight and Dynamic reconfigurability is a further enhancement to support update of hardware functions on-board
• Limitation of bus structure based dynamic reconfigurable SoC
• SoCWire
  - Flexible high-speed communication architecture
  - Support of adaptive macro-pipeline
  - Hot-plug ability
  - Suitable for dynamic reconfigurable systems
• Qualification of the system can be guaranteed
+ Isolates reconfigurable modules from the host system