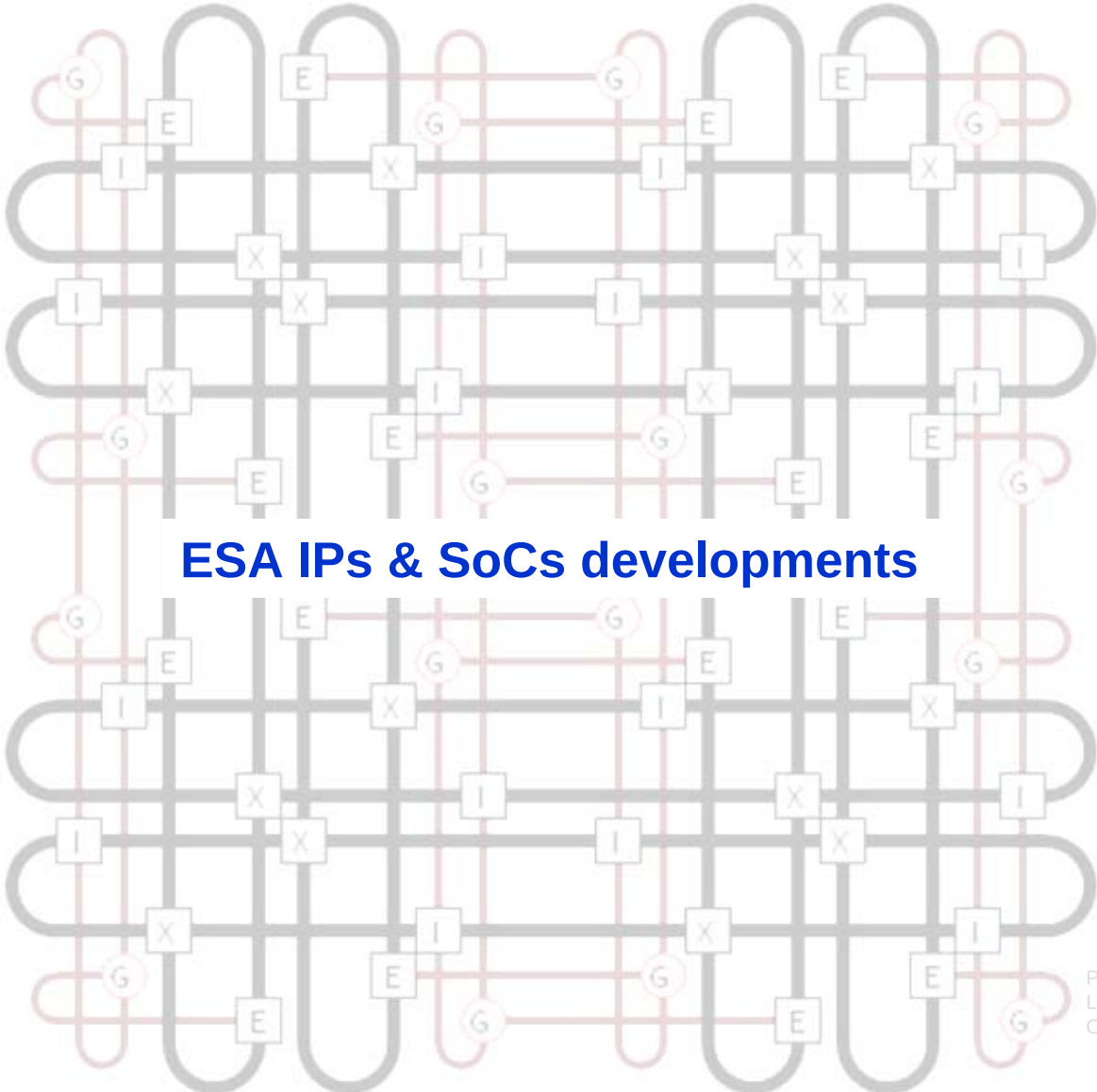


ESA IPs & SoCs developments

Picture courtesy of:
Lightwave Research Laboratory
Columbia University NY

Laurent Hili ESA / micro-electronics section

ESA IP cores portfolio

- Processor
  - Leon2 FT → Fault tolerant Sparc V8 architecture
- Data handling Interfaces
  - CAN → CAN B controller
  - 1553 → MIL-1553-B protocol, 3 modes Bus Controller (BC), Remote Terminal (RT), Bus Monitor (BM)
  - SpaceWire serial links (up to 400 Mbits/s)
    - SpaceWire-b → transceiver CODEC
    - SpaceWire-RMAP → Remote memory access protocol (RMAP)
    - SpaceWire-AMBA → SpaceWire with AMBA interface & RMAP protocol
- Telemetry and telecommand (CCSDS protocol)
  - PDEC → Packet Telecommand Decoder
  - PTCD → Packet Telecommand Decoder
  - PTME → Packet Telemetry Encoder

for more info please refer to ESA microelectronics WEB page, IP cores section:
http://www.esa.int/TEC/Microelectronics/SEMVWLV74TE_0.html#subhead2

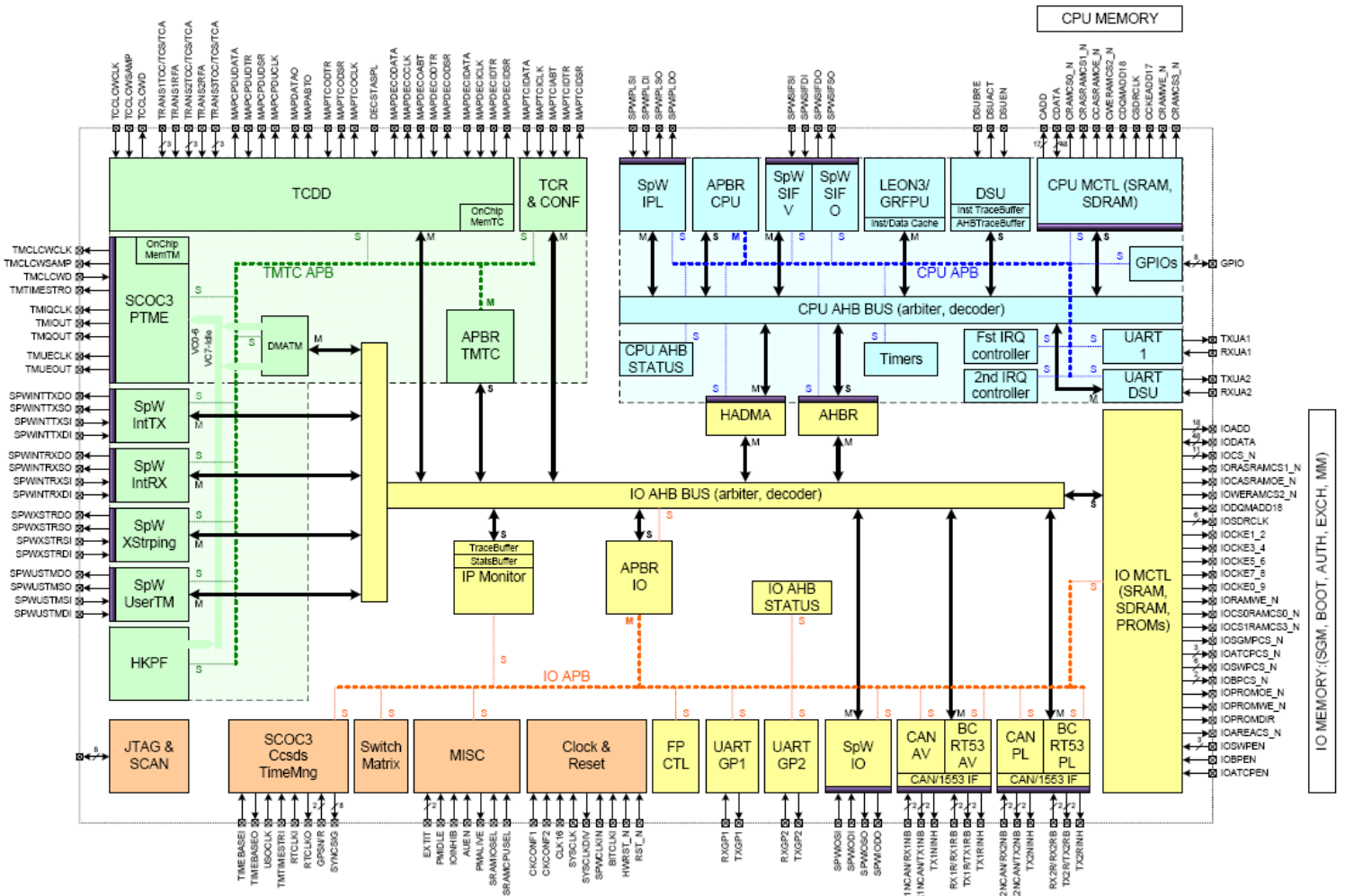
Processors developments

- On going activity
  - NGMP → Next Generation Microprocessor
    Leon4 FT multi core AMBA AHB (bus architecture)
    Contract awarded to Gaisler Aeroflex (Gothenburg / Sweden)
    Goals:
    - To demonstrate Performances > 400 MIPS
- On going pre-studies
  - MPP → Massive Parallel Processor
    Tile processor array (Network on Chip architecture)
    Goals:
    - To demonstrate performances > 1 GFlops
    - To demonstrate scalability (many cores)

    Contract awarded to Recore and Twente University (The Netherlands).
  - NGDSP → Next Generation Digital Signal Processor
    - To demonstrate performances > 1 GFlops
    - TI, Analog Device, Atmel solutions under evaluation

ESA SoC developments

Spacecraft Controller On Chip → SCOC3 (Astrium / France)



ESA SoC developments

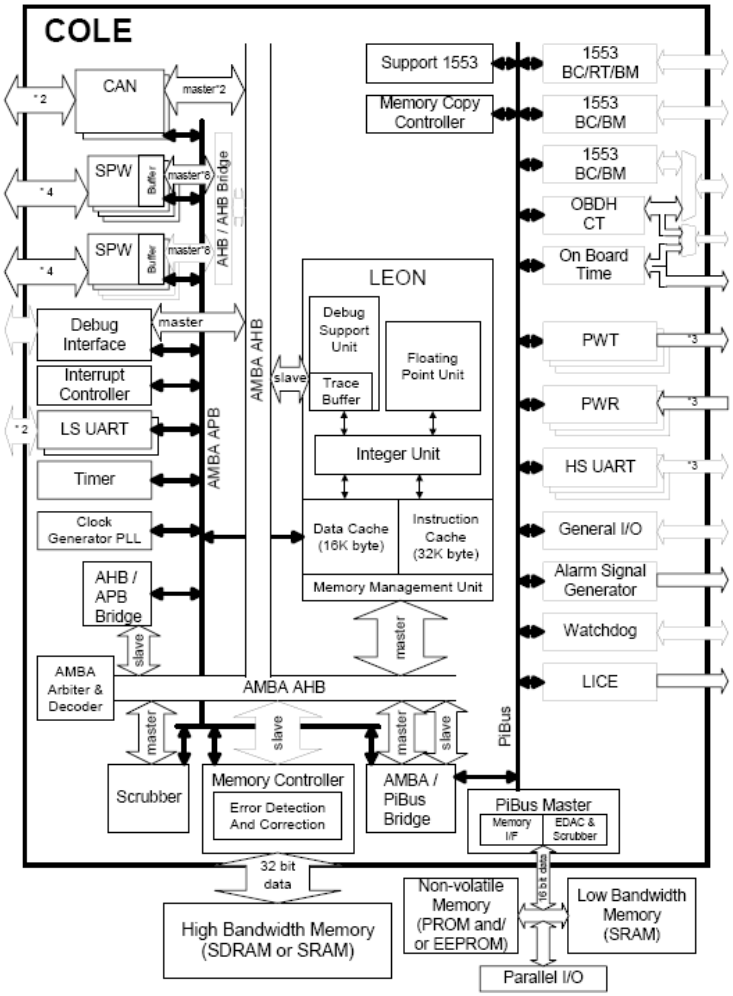
SCOC3

- SCOC3 is a system on chip for spacecraft control and data handling
- SCOC3 performs the following tasks
  - Attitude Orbital Control System (AOCS) → spacecraft main computer
  - Telemetry and telecommand (TM/TC) → compliant with CCSDS standard
  - House keeping, time and power management
- SCOC3 encompasses the following IPs blocks
  - A processing unit is built around a LEON3 FT processor with a floating point unit (GRFPU) and a memory controller communicating via a CPU-AHB AMBA bus (120 MHz / 100MIPS)
  - A set of IOs
    - UART
    - CAN
    - 1553 (Bus controller & remote terminal)
    - SpaceWire with RMAP controller
  - CCSDS TM/TC
    - Packet telemeasure encoder (PTME)
    - Telecommand decoder (TDCA)
  - CCSDS time generator

ESA SoC developments

COCOS (COmputerCOreSupport) I/O + **LE**ON2-FT processor = COLE

COLE (RUAG / Sweden)



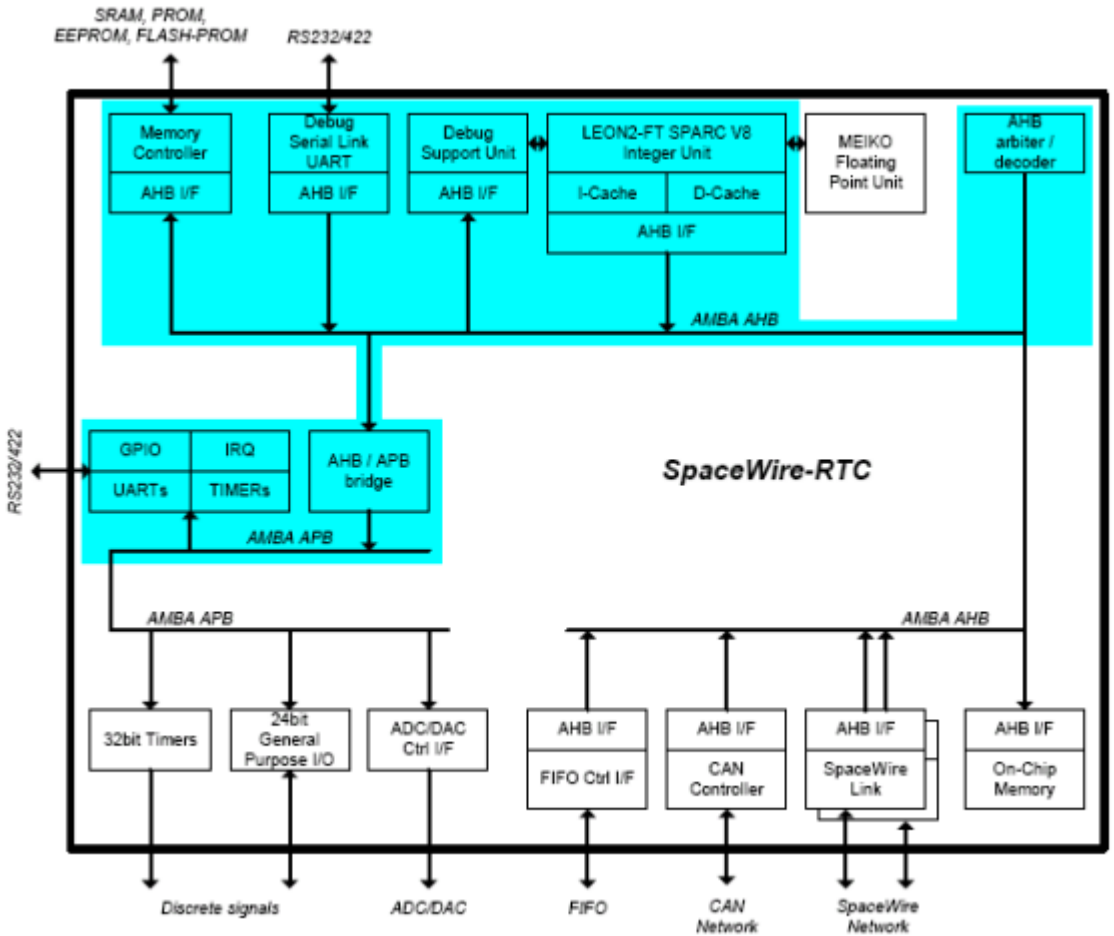
ESA SoC developments

COLE

- COLE encompasses the following IPs blocks
  - LEON2 FT processor with a floating point unit (Meiko) and a memory controller (100 MHz / 86 MIPS)
  - A set of IOs
    - Three MIL-STD-1553B bus interfaces
    - OBDH bus Central Terminal
    - Three PacketWire Receivers and Transmitters
    - Three High-Speed UART
    - General purpose I/O Interface with 12 I/Os
    - On Board Time (OBT) with synch. pulses
    - Alarm Signal Generator
    - Watchdog

ESA SoC developments

Remote Terminal Controller → RTC (RUAG / Sweden)



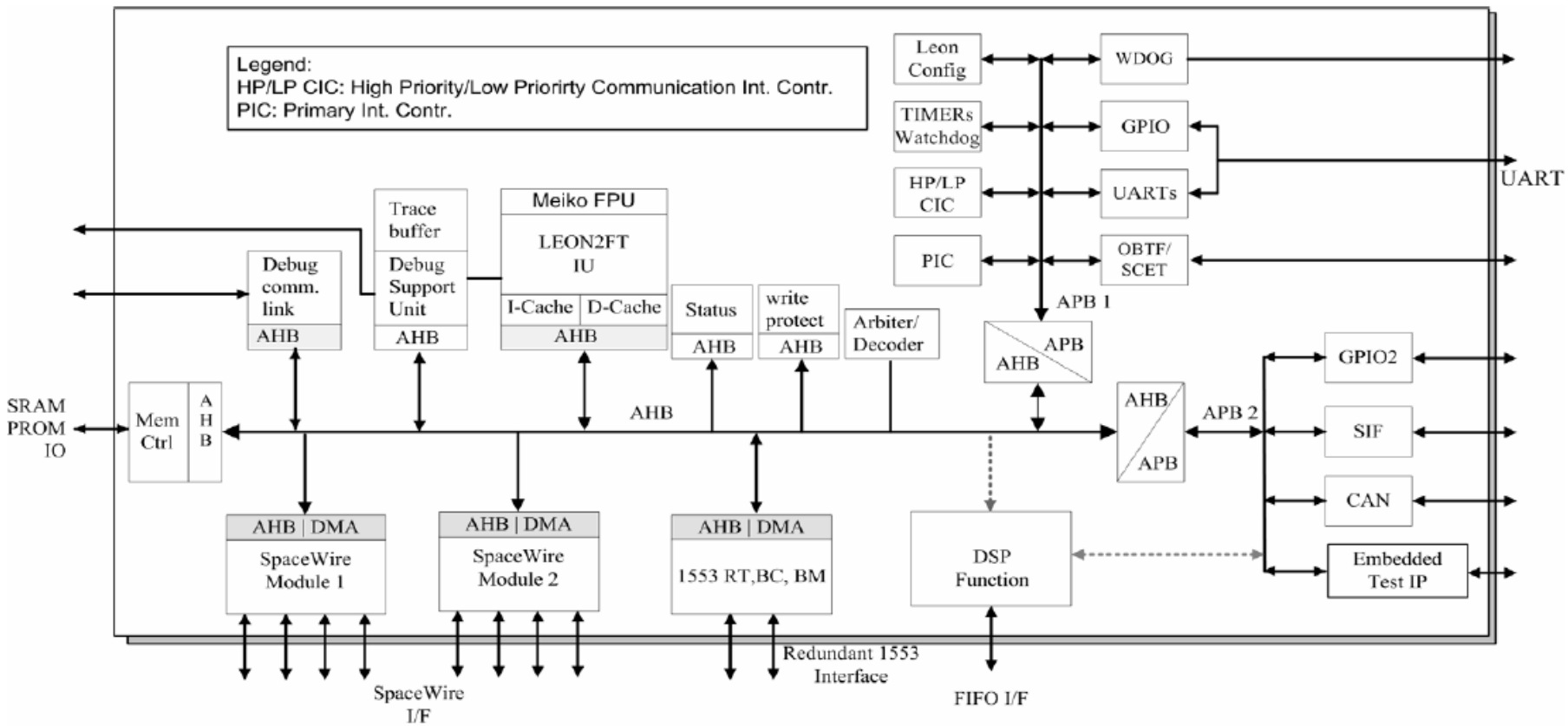
ESA SoC developments

RTC

- RTC is a remote terminal controller
- RTC performs the following tasks
  - Digital acquisitions
  - Timers & pulses generation
  - watchdog
  - Interfaces with AD / DA
- RTC encompasses the following IPs blocks
  - LEON2 FT processor with a floating point unit (Meiko) and a memory controller (50 MHz / 34 MIPS)
  - A set of IOs
    - General purpose I/O Interface with 24 I/Os
    - 2 UARTS
    - HurriCANe CAN core
    - 2 SpW CoDec with RMAP

ESA SoC developments

Multi-DSP/Micro-Processor → MDPA (Astrium / Germany)



ESA SoC developments

MDPA

- MDPA is a payload control processor scalable to multi-processors via SpaceWire
- MDPA performs the following tasks
  - High data rate payload telemetry / telecommand compliant with DVB-S (600 kbps in each direction)
- MDPA encompasses the following IPs blocks
  - LEON2 FT processor with a floating point unit (Meiko) and a memory controller (80 MHz / 70 MIPS)
  - A set of IOs
    - General purpose I/O Interfaces
    - 2 MIL-STD-1553B Interface Controller
    - UARTS
    - 1 HurriCANe CAN core
    - 8 SpaceWire interfaces

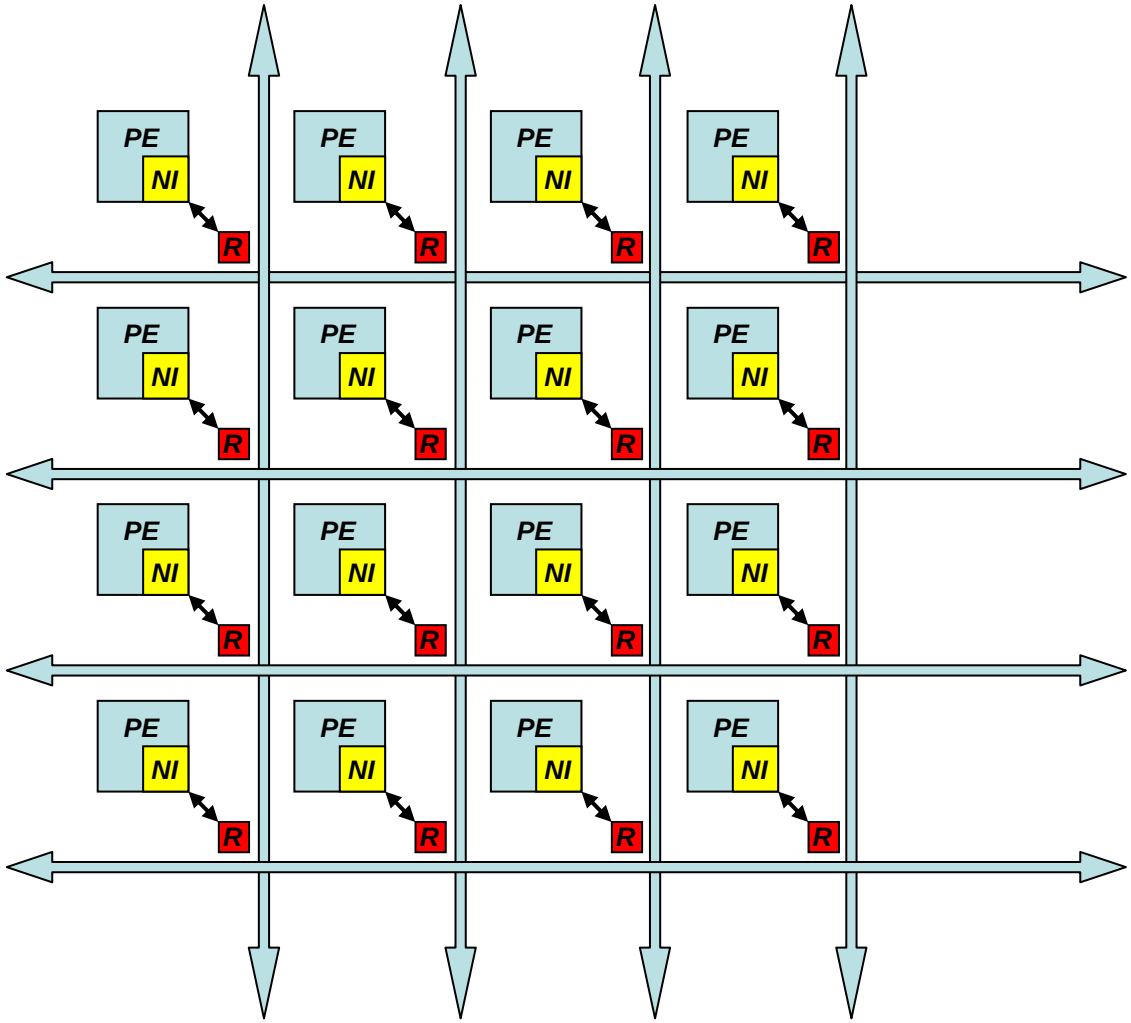
Trends and limitations in SoC design today

- Features embedded in SoCs tend to get more and more complex
- The number of IP blocks increases
- Bus based solutions (i.e AMBA –AHB) exhibit limitations:
  - Bus is a shared communication medium, therefore arbitration mechanisms are needed to attribute the bus resource
  - 1 master active at a time
  - Bus clock rate decreases as the number of IP blocks increases
  - Bus topology is not scalable when the number of peripherals increases
- Multi-layer bus architectures may alleviate some limitations mentioned above at the expense of extra complexity
- In modern sub-micron technologies interconnects dominate designs
  - Place & route, timing closure become tricky when number of IP blocks and bus data rates increase
  - Signal integrity issues with large synchronous parallel buses (crosstalk)
  - Performance (bus bandwidth) collapses when capacitive loads and number of IP blocks increases

Can NoC improve the situation ?

- Advantages
  - Point to point connection between IP blocks
    - Eases timing closure and signal integrity
    - Increases throughput thanks to limited capacitive load on each link
    - Eases the implementation of the GALS concepts (Globally Asynchronous Locally Synchronous)
  - Decoupling between processing units and communication interfaces can ease floor plan and place & route
  - Several masters can be active at the same time
  - Serial links or serial/parallel links can ease place & route compared to large synchronous parallel buses
- Drawbacks
  - Latency (routers hops) can be an issue in time critical applications
    - Latency issue can be overcome if shortcuts can be established between remote nodes
  - Performance may collapse if applications / algorithms don't exhibit a certain degree of locality
    - Access to remote memories out of the processing node may degrade performance
    - Communication links with the processing unit and immediate neighbours shall be maximised
  - Traffic modelling tools and network dimensioning might be more complex than traditional well known bus based architectures

Typical 2D mesh NoC topology



Legend:
PE → Processing Element
NI → Network Interface
R → Router

Future perspectives

- On going ESA TRP contract to develop the future Space ASIC technology (ST 65nm node)
- Future DSM technology will require the development of a specific backbone IPs interconnect fabric (NoC)
- The NoC may allow a clear decoupling between processing units and communication
- The decoupling may alleviate some of the cumbersome problems predominant in DSM technologies
  - Timing closure
  - Signal integrity
  - Floor plan, Place & Route

Future perspectives

- Despite few drawbacks such as latency and extra complexity (routers) advantages overcome drawbacks when targeting DSM technologies (65nm and below)
- The tremendous integration capacity offered by DSM technologies will allow redundancy (spare nodes)
- The use of NoCs for Space applications will require further investigation in the following fields:
  - Time predictability
  - QoS
  - Fault tolerance
  - Redundancy
  - Reliability
- Scalability → convergence between on / off chip network ?
- Which programming model for many cores applications ?

ANY QUESTIONS ?

ENJOY !!! ☺