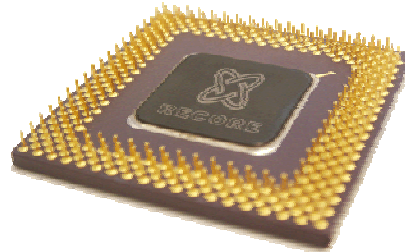


September 17, 2009

Scalable programmable many-core SoC architectures using NoC technology



Gerard Rauwerda
Recore Systems BV

P.O. Box 77, 7500 AB,
Enschede, The Netherlands
☎ +31 53 4753 000
☎ +31 53 4753 009
info@recoresystems.com

www.recoresystems.com




Agenda

- Introduction – Recore Systems
- Multi-core reconfigurable SoC
- CRISP – General Stream Processor template
- MPPB – Massively Parallel Processor Breadboarding

© 2009 Recore Systems BV

2

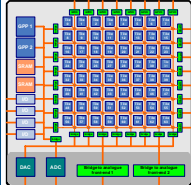
Confidential



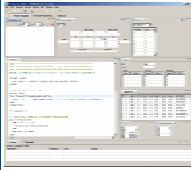
Products and services providing complete solutions

- Reconfigurable multi-core designs
 - Tailored for application domains
- Hardware IPs
 - Montium®, Xentium™ and Mementum™
 - Network-on-Chip, interfaces, bridges, ...
- Design tools
 - Compilers, simulators, IDEs, ...
- DSP applications
 - Kernel libraries (FFT, FIR, DCT, Viterbi, ...)
 - COTS (wireless, broadcasting, multimedia, ...)
 - Custom engineering services
- Digital radio/TV platform
 - One-chip solution for DMB, DAB(+), ...

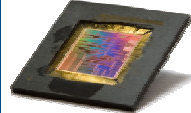
*64-core
for
high-end
stream
processing*



*Sensation
Suite
IDE*




*Silicon
Proven
Montium
4-core*



© 2009 Recore Systems BV


3

Confidential



Agenda


- Introduction – Recore Systems
- Multi-core reconfigurable SoC
- CRISP – General Stream Processor template
- MPPB – Massively Parallel Processor Breadboarding



© 2009 Recore Systems BV

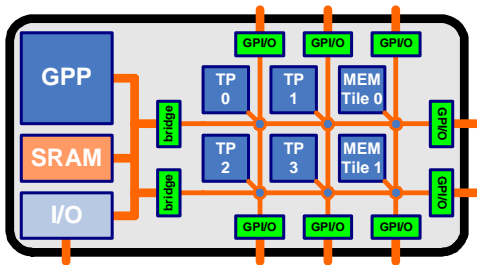
4

Confidential

 **RECORE**

Multi-core architecture for streaming DSP applications


- General Purpose Processor (GPP) subsystem
 - Control processor
 - Operating System / GUI
 - Configuration management
 - Highly irregular code
 - E.g. ARM or Leon processor(s)
- Reconfigurable fabric
 - Matrix of reconfigurable cores
 - Domain specific
 - Network-on-Chip
 - Distributed memories
 - Distributed control



© 2009 Recore Systems BV

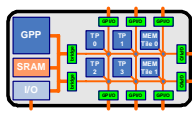
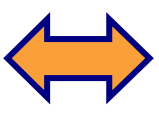
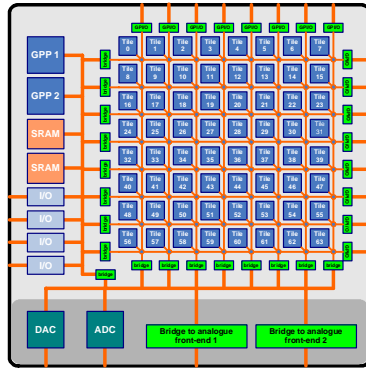
5

Confidential

 **RECORE**

A truly scalable architecture

- A single platform for all stream processing applications
- A single design methodology
- Scalability by virtue of
 - Packet switched Network-on-Chip
 - Distributed memories
 - Distributed control


*Small multi-core platforms for low-end applications
(e.g. consumer, automotive)*

*Large many-core platforms for high-end applications
(e.g. medical, defense)*

© 2009 Recore Systems BV

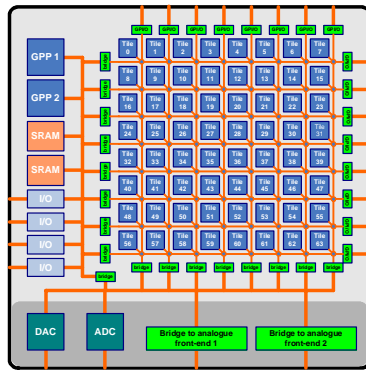
6

Confidential

 **RECORE**

Heterogeneous multi-core


- Scalability by virtue of
 - Packet switched Network-on-Chip
 - Distributed memories
 - Distributed control
- Xentium™ processing tile
 - Block floating-point processing
 - VLIW-like DSP
 - Autonomous program fetching
 - Streaming communication services
- Mementum™ memory tile
 - Embedded SRAM-based memory
 - Dynamically reconfigurable
 - Random access memory
 - FIFO/LIFO/cyclic buffers
 - (De-)interleaving



- Scalability on different levels
 - Cores
 - Systems-on-Chip
 - Boards
 - Cabinets


© 2009 Recore Systems BV

10 Confidential

 **RECORE**

Agenda

- Introduction – Recore Systems
- Multi-core reconfigurable SoC
- CRISP – General Stream Processor template
- MPPB – Massively Parallel Processor Breadboarding



© 2009 Recore Systems BV

11 Confidential

General Stream Processor architecture

- Modular approach to prove concepts
 - Multiple dies in a chip
 - Multiple chips on a PCB
 - Multiple PCBs in a cabinet
- Multichip modules
 - General Purpose die
 - 32-bit General Purpose Processor
 - Various I/Os
 - Reconfigurable die
 - Reconfigurable Tile Processors
 - Hard macro
 - Smart Memory Tiles
 - Network-on-Chip
 - Various (high-speed) I/Os

The diagram illustrates the General Stream Processor architecture. It consists of two main components: a General Purpose Die and a Reconfigurable Die. The General Purpose Die contains a 32-bit GPP, Logic, RAM, ROM, CACHE, and an ADC analog block. It has various I/Os including GPIO, SSC, EBI, ADC IF, SPI0, SPI1, OSC, and JTAG. The Reconfigurable Die is a grid of modules including Smart Memory 1, Smart Memory 2, and various Reconfigurable Tile Processors (MCP, SSC, JTAG, TEST). It also has I/Os like SSC, MCP, C2C, JTAG, and TEST.

© 2009 Recore Systems BV

12

Confidential


The CRISP PCB contains at least two multi-chip modules for prototyping

The diagram shows the CRISP PCB layout, which contains at least two multi-chip modules for prototyping. Each module consists of a General Purpose Die and a Reconfigurable Die, connected by a C2C interface. The General Purpose Die is identical to the one in the previous slide. The Reconfigurable Die is also identical. The modules are connected to each other and to the PCB I/Os.

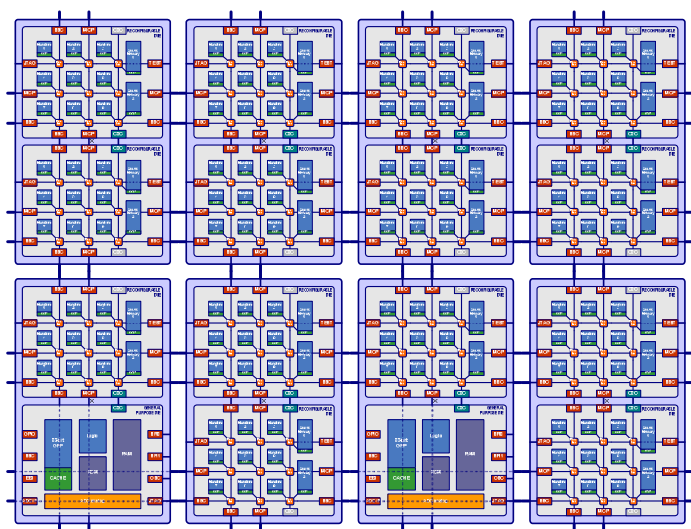
© 2009 Recore Systems BV

13

Confidential


 **RECORE**

Larger systems can be prototyped similarly

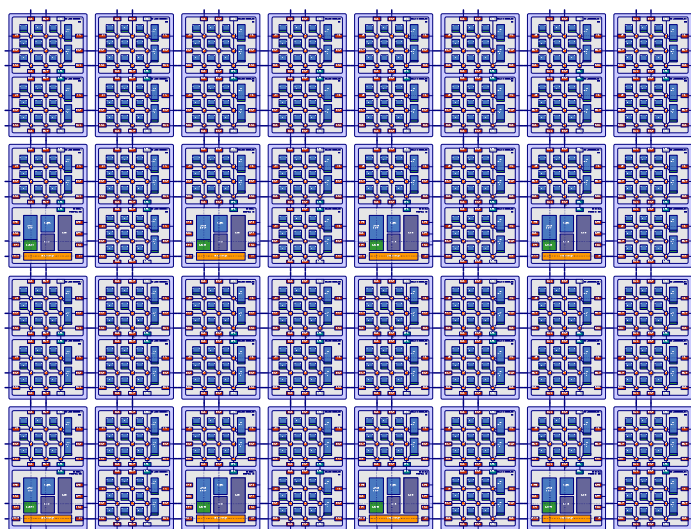


© 2009 Recore Systems BV

14 Confidential

 **RECORE**

The bigger picture...



© 2009 Recore Systems BV

15 Confidential


 **RECORE**

Agenda

- Introduction – Recore Systems
- Multi-core reconfigurable SoC
- CRISP – General Stream Processor template
- MPPB – Massively Parallel Processor Breadboarding

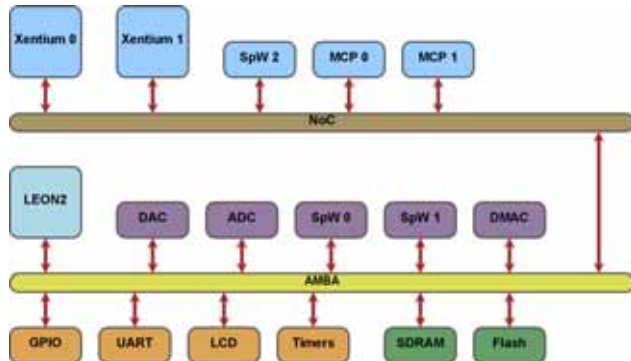
© 2009 Recore Systems BV

Confidential

 **RECORE**

MPPB architecture overview


- Processing components
 - ✓ LEON2 processor
 - ✓ Xentium™ processing tile
- On-chip communication
 - ✓ AMBA bus system
 - ✓ Network-on-Chip



The diagram illustrates the MPPB architecture. It features two main horizontal buses: a top brown bus labeled 'NOC' (Network-on-Chip) and a bottom yellow bus labeled 'AMBA' (Advanced Microcontroller Bus Architecture). Above the NOC bus are five components: Xentium 0, Xentium 1, SpW 2, MCP 0, and MCP 1. Below the NOC bus and above the AMBA bus are six components: LEON2, DAC, ADC, SpW 0, SpW 1, and DMAC. Below the AMBA bus are six peripheral components: GPIO, UART, LCD, Timers, SDRAM, and Flash. Bidirectional red arrows connect each component to its respective bus, indicating communication flow.

© 2009 Recore Systems BV

Confidential




Interfaces SpW-NoC

- Purpose
 - Provides standard interface for space systems
- Features
 - Network interface
 - Using ESA SpW-interface as back-end
 - Memory mapped transmit and receive buffers
 - Memory mapped status and configuration registers
 - Minimum link speed (FPGA): 100 Mbit/s

© 2009 Recore Systems BV

18 Confidential

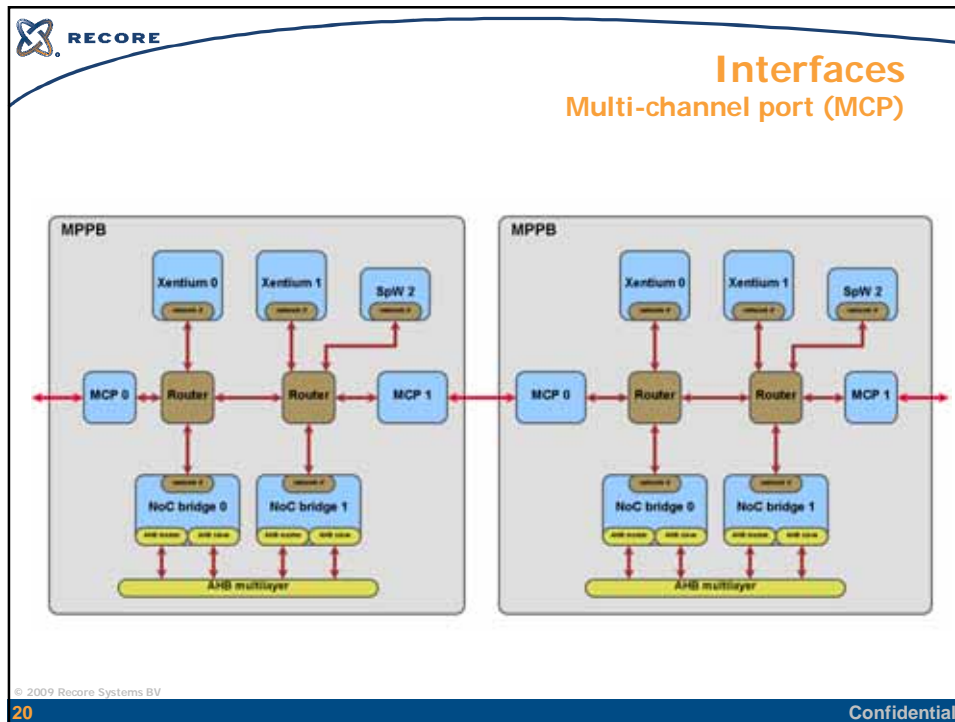


Interfaces Multi-channel port (MCP)

- Purpose
 - Connecting two chips via the NoC
 - Increase resources (interfaces, processors and memory)
- Features
 - Transparently forwards the NoC flits
 - Minimum throughput: 1 Gbit/s
 - Performance has been verified on FPGA

© 2009 Recore Systems BV

19 Confidential



How can we help you?