Scalable programmable many-core SoC architectures using NoC technology

Agenda

- Introduction – Recore Systems
  - Multi-core reconfigurable SoC
  - CRISP – General Stream Processor template
  - MPPB – Massively Parallel Processor Breadboarding
**Products and services providing complete solutions**

- Reconfigurable multi-core designs
  - Tailored for application domains
- Hardware IPs
  - Montium®, Xentium™, and Membium™
  - Network-on-Chip, interfaces, bridges, ...
- Design tools
  - Compilers, simulators, IDEs, ...
- DSP applications
  - Kernel libraries (FFT, FIR, DCT, Viterbi, ...)
  - COTS (wireless, broadcasting, multimedia, ...)
  - Custom engineering services
- Digital radio/TV platform
  - One-chip solution for DMB, DAB(+), ...

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Multi-core architecture for streaming DSP applications

- General Purpose Processor (GPP) subsystem
  - Control processor
    - Operating System / GUI
    - Configuration management
    - Highly irregular code
  - E.g. ARM or Leon processor(s)

- Reconfigurable fabric
  - Matrix of reconfigurable cores
  - Domain specific
  - Network-on-Chip
  - Distributed memories
  - Distributed control

A truly scalable architecture

- A single platform for all stream processing applications
- A single design methodology
- Scalability by virtue of
  - Packet switched Network-on-Chip
  - Distributed memories
  - Distributed control

Small multi-core platforms for low-end applications (e.g. consumer, automotive)

Large many-core platforms for high-end applications (e.g. medical, defense)
Heterogeneous multi-core

- Scalability by virtue of
  - Packet switched Network-on-Chip
  - Distributed memories
  - Distributed control
- Xentium™ processing tile
  - Block floating-point processing
  - VLIW-like DSP
  - Autonomous program fetching
  - Streaming communication services
- Memtium™ memory tile
  - Embedded SRAM-based memory
  - Dynamically reconfigurable
    - Random access memory
    - FIFO/LIFO/cyclic buffers
    - (De-)interleaving
- Scalability on different levels
  - Cores
  - Systems-on-Chip
  - Boards
  - Cabinets

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General Stream Processor architecture

- Modular approach to prove concepts
  - Multiple dies in a chip
  - Multiple chips on a PCB
  - Multiple PCBs in a cabinet

- Multichip modules
  - General Purpose die
    - 32-bit General Purpose Processor
    - Various I/Os
  - Reconfigurable die
    - Reconfigurable Tile Processors
      - Hard macro
      - Smart Memory Tiles
      - Network-on-Chip
      - Various (high-speed) I/Os

The CRI SP PCB contains at least two multi-chip modules for prototyping
Larger systems can be prototyped similarly

The bigger picture...
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**MPPB architecture overview**

- Processing components
  - LEON2 processor
  - Xentium™ processing tile
- On-chip communication
  - AMBA bus system
  - Network-on-Chip
Interfaces
SpW-NoC

- **Purpose**
  - Provides standard interface for space systems

- **Features**
  - Network interface
  - Using ESA SpW-interface as back-end
  - Memory mapped transmit and receive buffers
  - Memory mapped status and configuration registers
  - Minimum link speed (FPGA): 100 Mbit/s

Interfaces
Multi-channel port (MCP)

- **Purpose**
  - Connecting two chips via the NoC
  - Increase resources (interfaces, processors and memory)

- **Features**
  - Transparently forwards the NoC flits
  - Minimum throughput: 1 Gbit/s
  - Performance has been verified on FPGA