Network on Chip round table
European Space Agency, ESTEC
Noordwijk / The Netherlands
17th and 18th of September 2009

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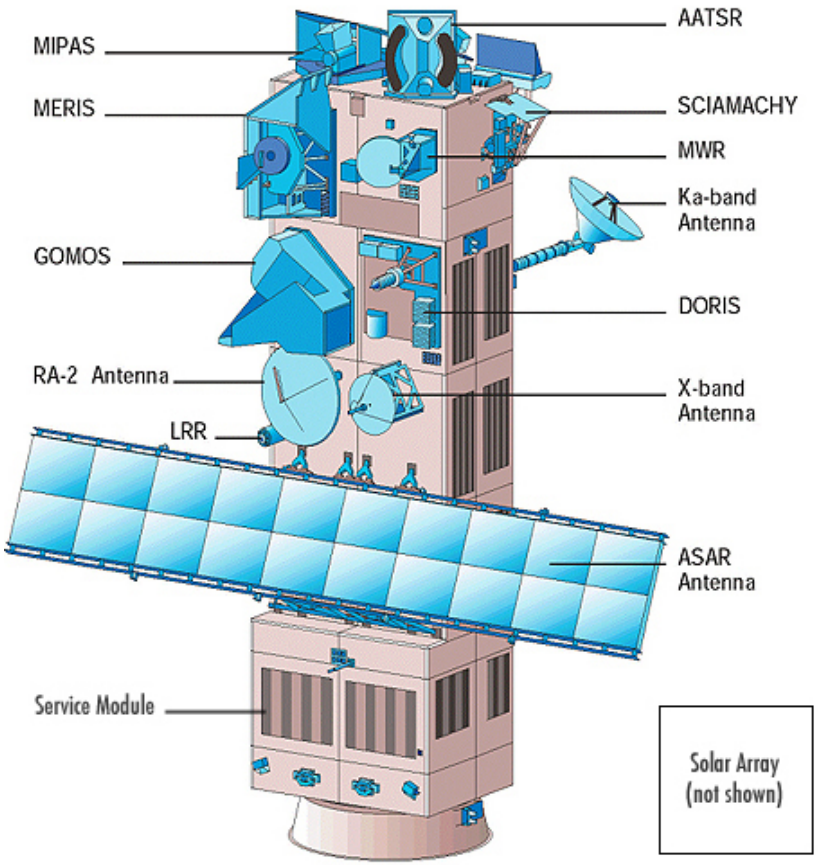
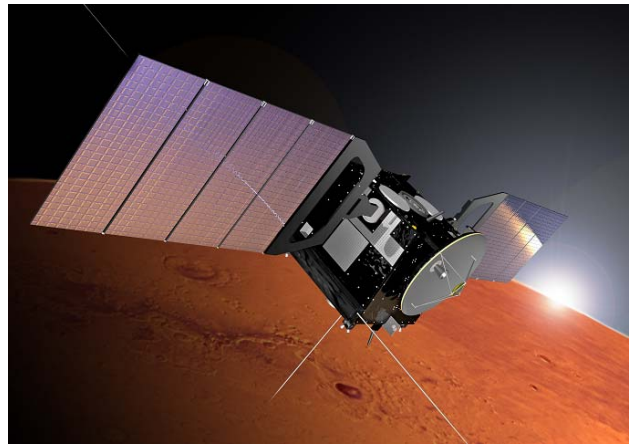
The European Space Research and Technology Centre (ESTEC)


MIPAS
MERIS
GOMOS
RA-2 Antenna
LRR
Service Module
AATSR
SCIAMACHY
MWR
Ka-band Antenna
DORIS
X-band Antenna
ASAR Antenna
Solar Array (not shown)



Overall goals : Avionics

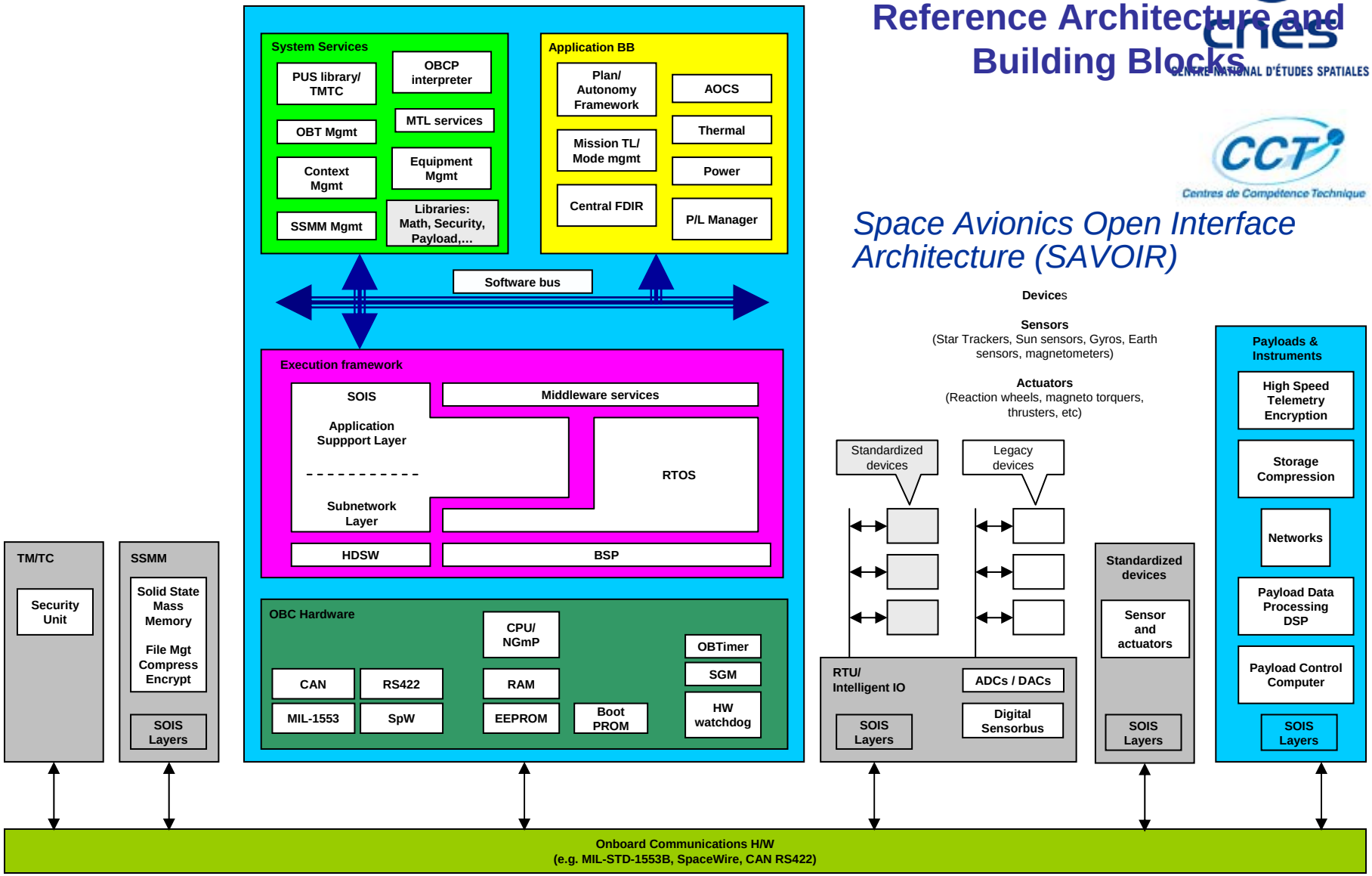
The Avionics sub-system corresponds to about 60% on the overall development costs for a satellite.

Therefore, ESA is paying special attention to means allowing to decrease these costs by:

- Defining reference architectures, e.g. common to a series of missions, for instance Earth Observation, Science and Exploration missions
- Standardising interfaces, developing communication services and protocols
- Fostering re-use of building blocks
- Developing tools and methodologies for composing a system from already validated building blocks.

Reference Architecture and Building Blocks

Space Avionics Open Interface Architecture (SAVOIR)



Reference Architectures: Modular Data Systems

Already in the 90s, it appeared clearly that a generic interface would be very useful on-board spacecraft, in order to ease the interconnection of:

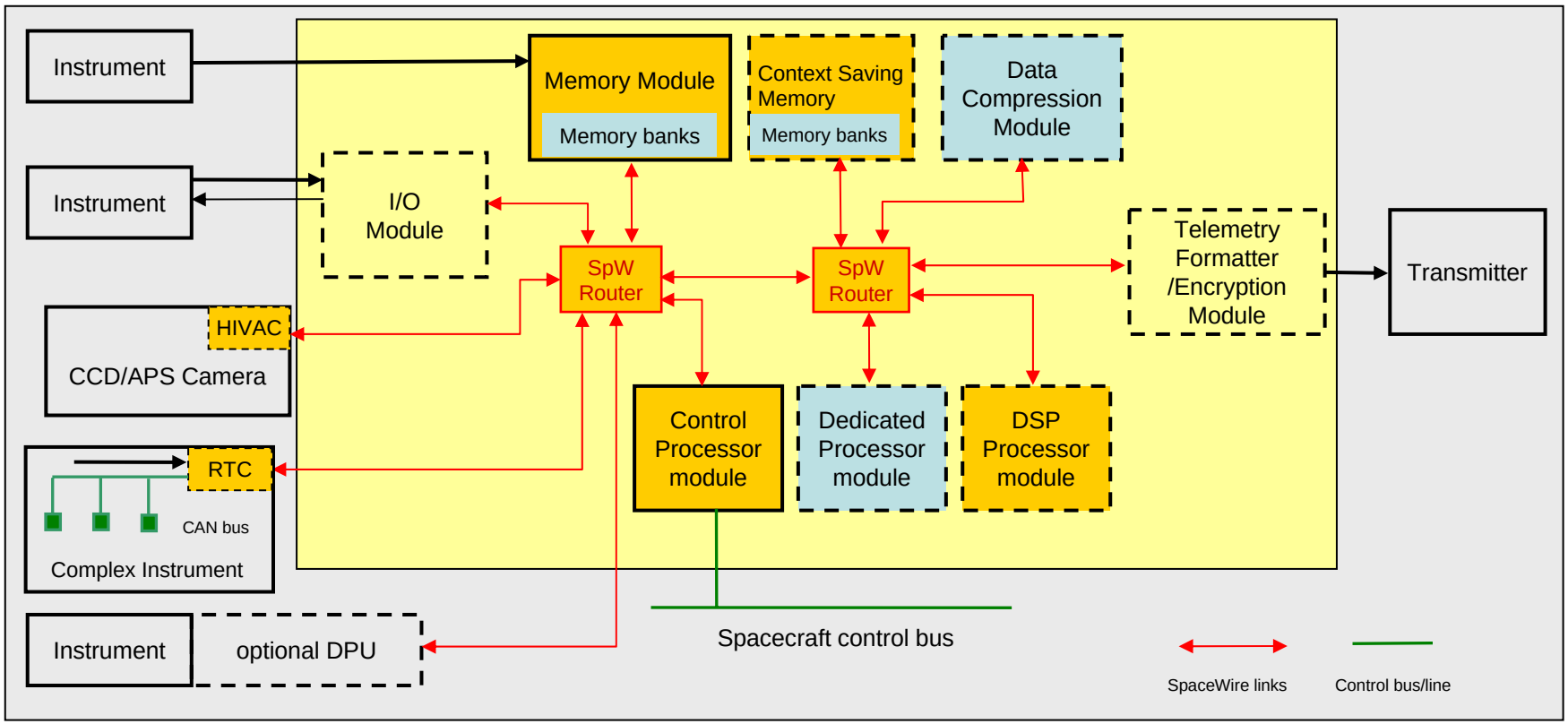
- Sensors
- Mass-memories
- Processing units, and
- Downlink telemetry sub-systems.

High speed Serial links in contrast to parallel interfaces have been selected due to their potential of constituting an homogeneous solution to interconnect components, board and units.

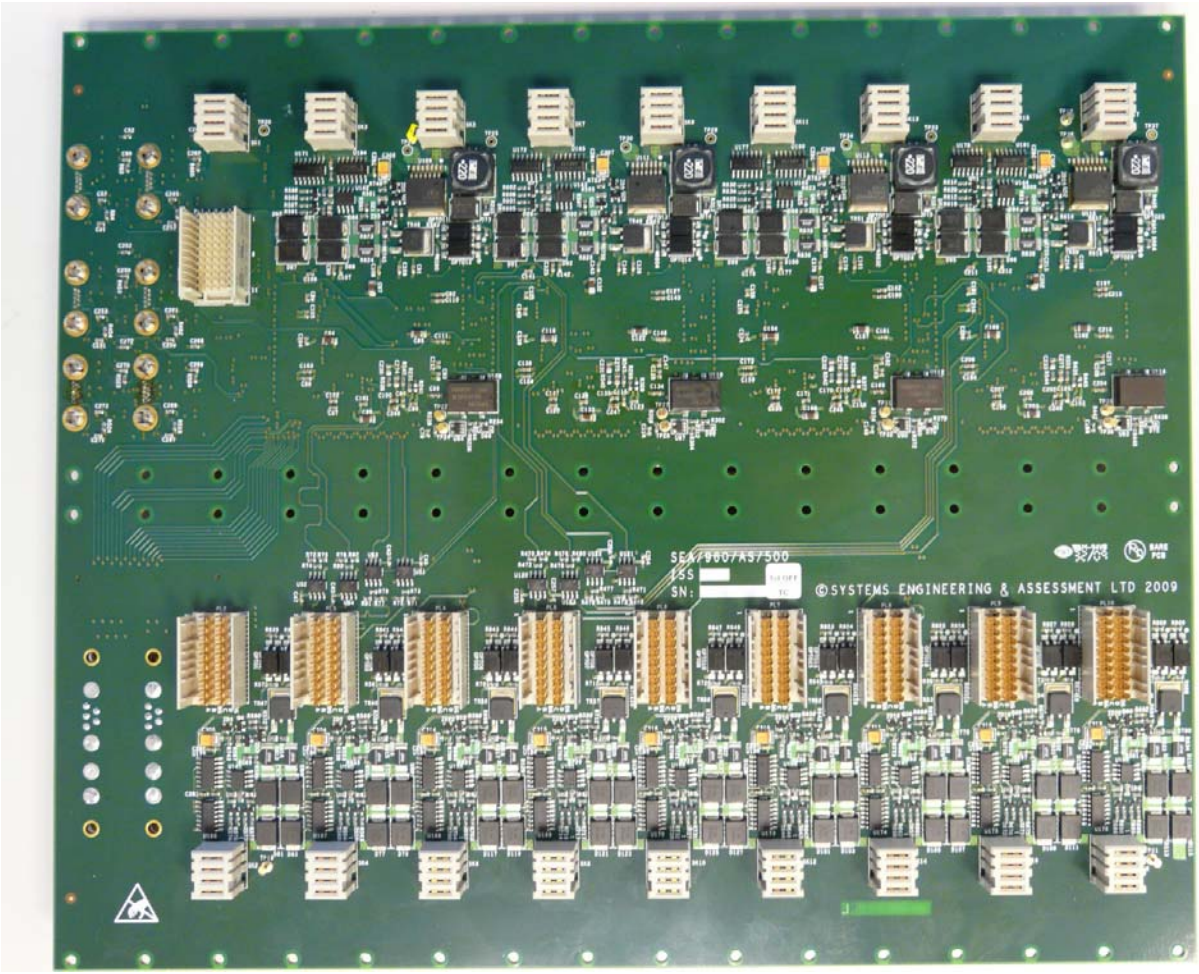
They allowed as well to define a reference architecture with <u>native modularity and scalability</u>.

Reference Architectures: Modular Payload Data Handling System

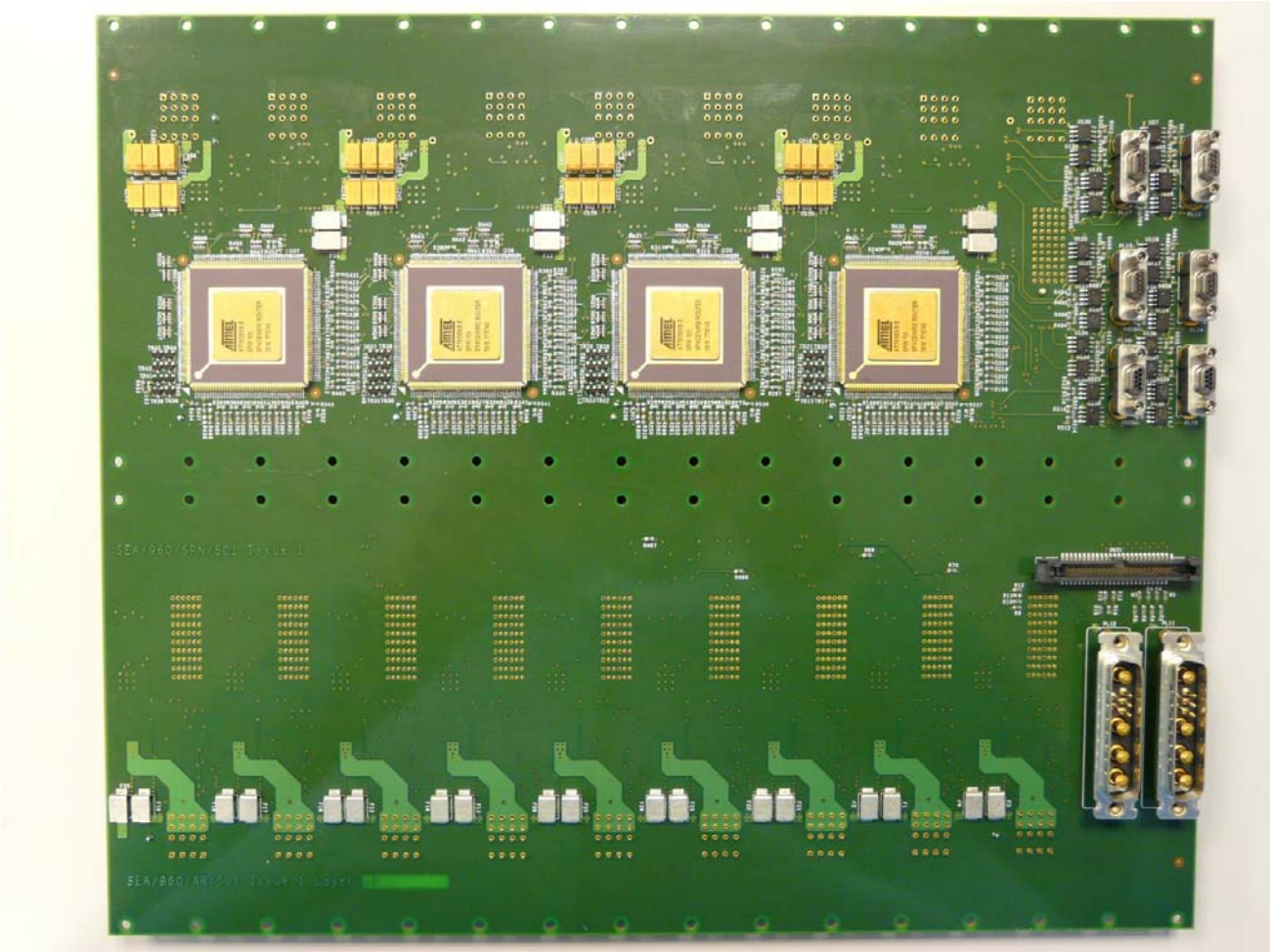
Architecture used by ESA as a reference for medium-range Data Handling Systems and the definition SpaceWire devices (SpW Router, SpW RTC, SMCS-SpW, …)



Backplane PCB - front



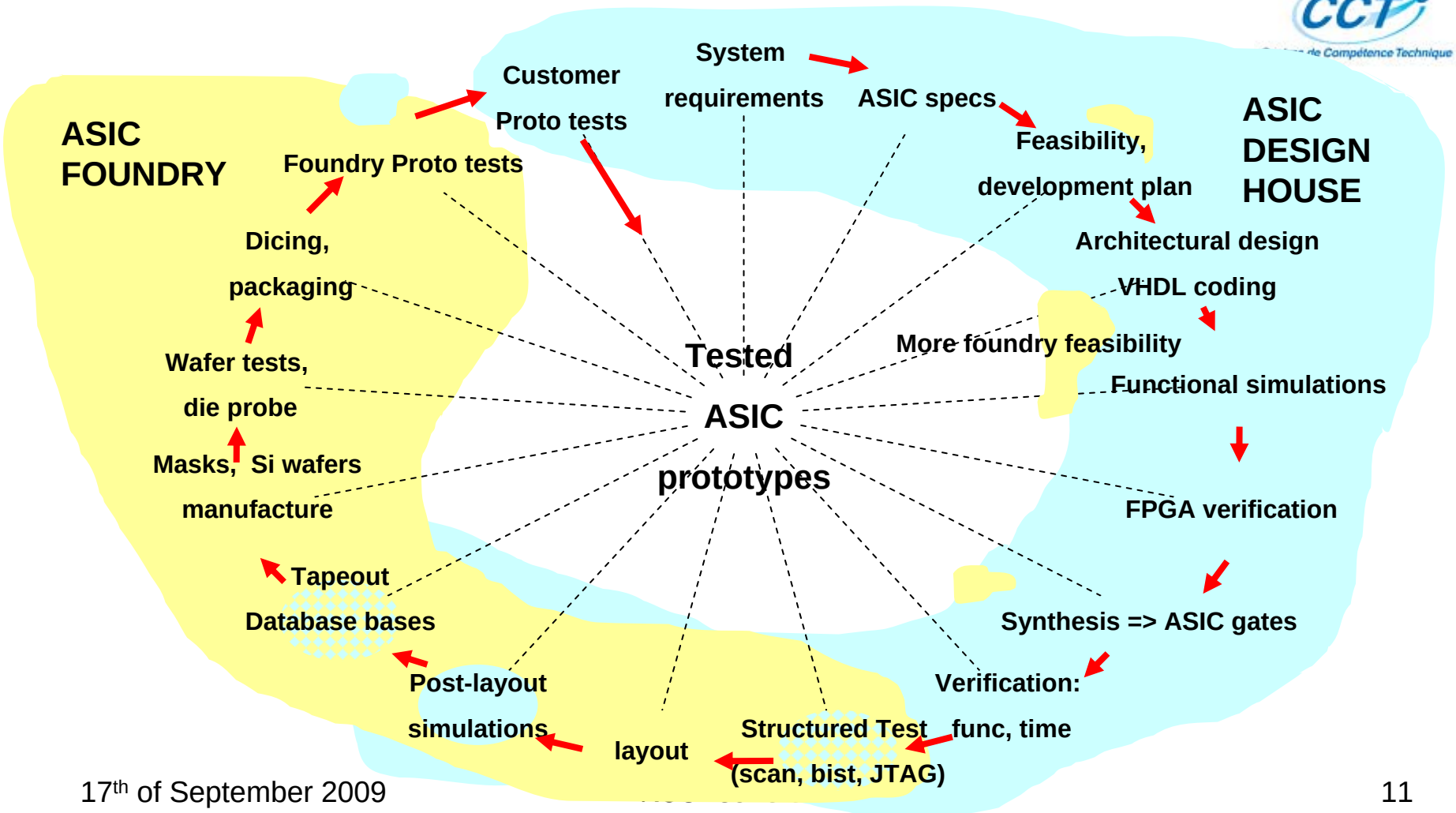
Backplane PCB - back



Challenges of space VLSIs

- Make best use of DSM technologies, providing
  - Higher speed
  - Allow to integrate complex systems on one chip
- Bound development times
  - Trend towards multi-year (2/3 … 5/7) development periods
- Define and validate new development paradigms
  - SoCs based on IP cores
  - Foster reuse of existing designs
  - Architectural design and HW/SW co-design

……. While keeping reliability and availability figures highest

Challenges of space SoCs

SoC-ASIC developments: complex design flow