CENTRE NATIONAL D'ÉTUDES SPATIALES

Why NoC for Space?

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Purpose

➢ ***Neither a NoC tutorial (it will be done later), Nor NoC design challenges and solution presentation, nor …***

➢ ***But a short look at***

- Trends (nanoelectronics industry and embedded systems for space applications)
- Some DSM reliability challenges
- NoC architecture opportunities to manage DSM reliability issues

➢ ***As a kind of introduction for this Round table***

➢ ***Coming from DSM FA / Reliability word (not a NoC specialist)***

Outline

- ***Few words on CCT MCE***
- ***Trends***
  - Moore's law
  - Space needs
  - Facing the integration consequences: from SoC to NoC
- ***DSM reliability challenges***
  - Lifetime issue
  - Noise margin issue
  - Manageable
- ***NoC an opportunity for high reliability***
  - Intrinsic NoC advantage
  - Using the flexibility of NoC
- ***Conclusion***

CCT MCE at a glance

➢ *Origin (1998)*

- Corporate network on many space related techniques (ie MCE, EdB)
- Maintain, develop and advantage skills
- Widely opened to other company dealing with space applications or with the core activity of a specific CCT (electronic Components and MEMS for CCT MCE).

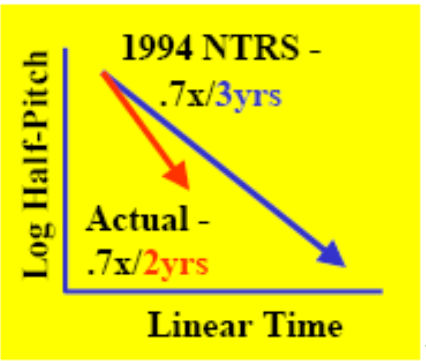
➢ *Objectives*

- Increase member competences by technical seminar, workshops and tutorials like this round table CCT MCE co organize with ESA;
- Mutualize expertise, Identify and put to light existing skills in and out CNES;
- Bring to members the outstanding studies and developments they can use;
- Disseminate the outstanding studies and developments made by spatial sector to other sectors;
- Give key information to prepare the future

Moore's Law

Scaling Calculator +

Cycle Time:



0.7x 0.7x

250 -> 180 -> 130 -> 90 -> 65 -> 45 -> 32 -> 22 -> 16

0.5x

N-1 N N+1

Area ↓

Speed ↑

Power ↓

Cost ↓

* CARR(T) = Compound Annual Reduction Rate (@ cycle time period, T)

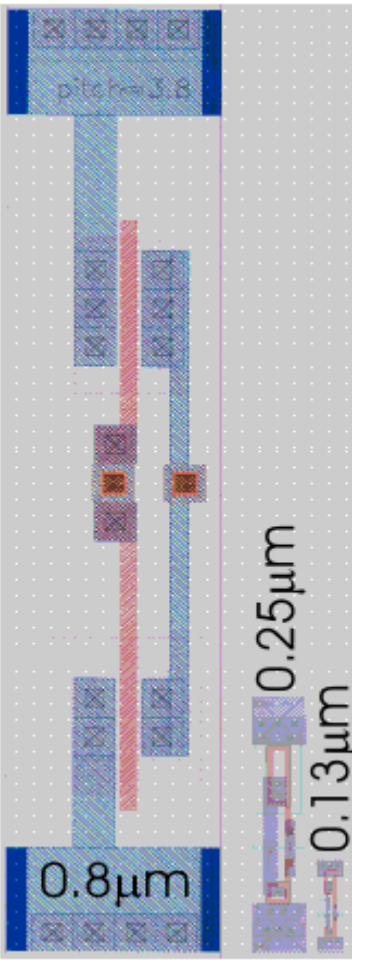
Cycle Time (T yrs):

*CARR(T) =

[(0.5)^(1/2T yrs)] - 1

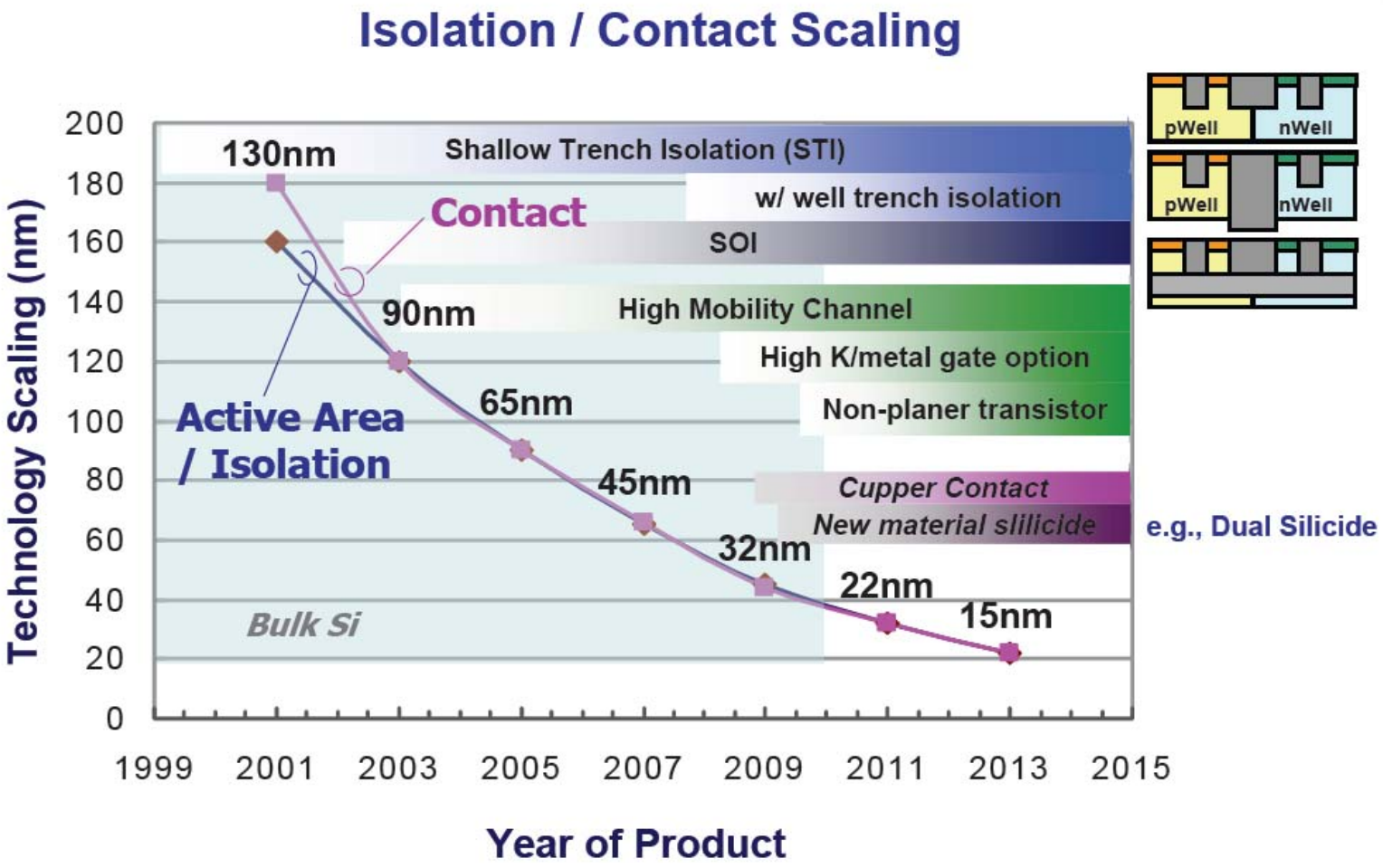
CARR(3 yrs) = -10.9%

CARR(2 yrs) = -15.9%



(DRAM M1 Example)

Nanotechnology trends



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Technology scaling and road map / Koji Miyamoto

- Exemple: Multicore
1 Bt / core

- Scaling of semiconductor creates a true SoC (complete electronic system including all its periphery and interfaces on a single die)

Space needs

- ***Space is user of nanoelectronic technology***
  - Use of available technology
  - Take advantage of technology evolution
- ***Specific constraints***
  - Environment (radiation)
  - Long term use (telecom …)
  - Out of repair (orbit)
  - Weight and power consumption
- ***… and wish list***
  - More and more integration (Processor core, Memory: RAM and flash or MRAM for all, IOs interfaces, Clock generators (PLLs): 10MHz external => 1Ghz internal, Control and FDIR functions: WDG, power management, reconfiguration …
  - Jean Louis' dream …

Jean-Louis dream

- ***If I have a big microcontroller including:***
  - The processor core: SPARC with FPU
  - Enough speed memory: 16Mbytes upset protected
  - Clock generator: internal PLL
  - 6 high speed serial bus (1Gb/s spacewire ??) with internal network gateway
  - Internal WDG
  - Internal power management and supervisor
  - Low power
- ***I could build a computing node in a chip..***
- ***I could build new architectures…***
  - Multinode architecture: array, farm, hypercube
  - Easy to use and upgradable
  - Redundancy
- ***Is the T9000 transputer concept from INMOS reborn ?***

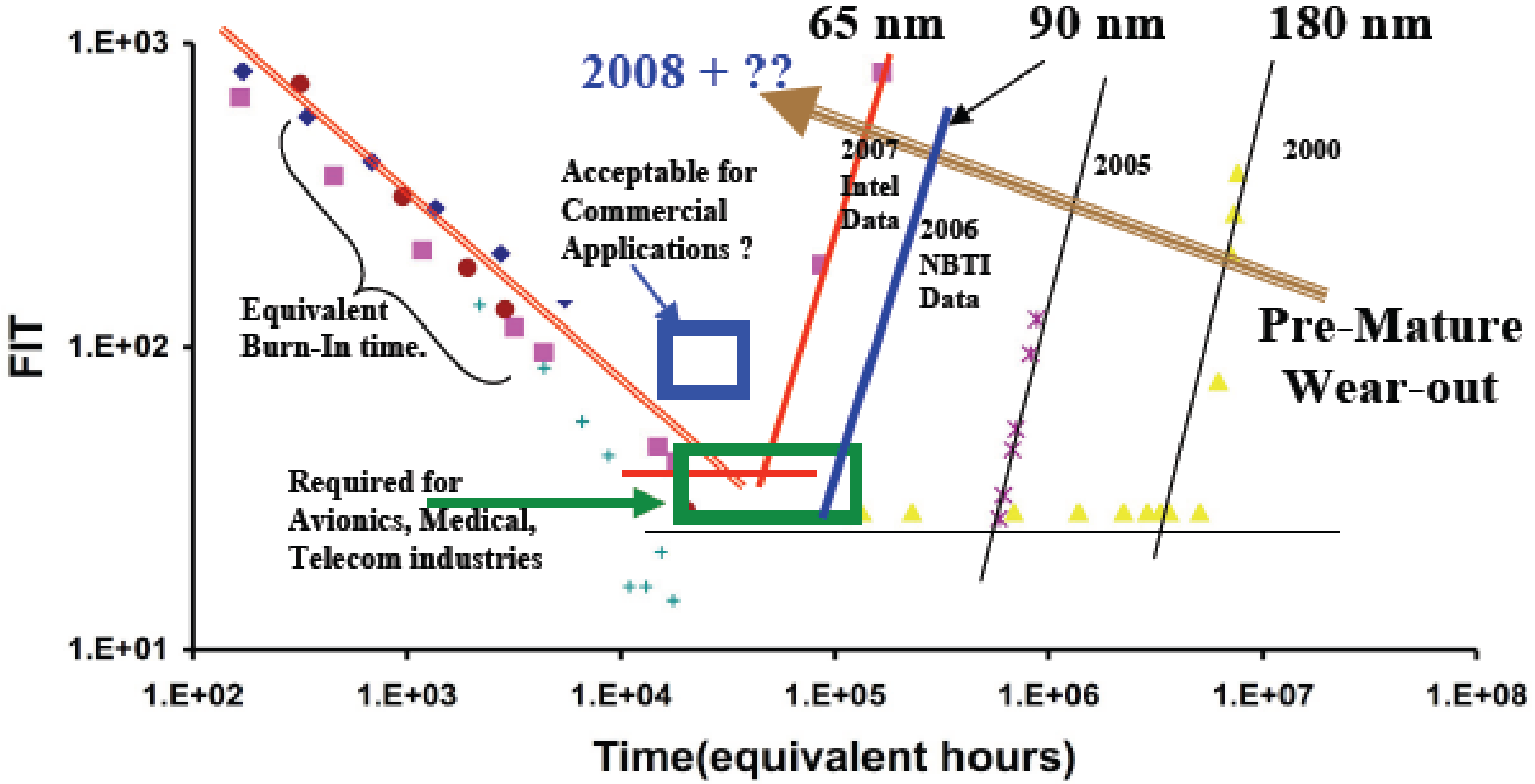
From SoC to NoC (1)

- ***SoC architecture issues***
  - *Communication between blocks is bus based in SoC*
  - *Bus is shared between internal blocks (Memory, DSP, ALU ….) and become a bottleneck*
  - *High speed Synchronous behavior is a nightmare that challenges clock tree design, triggers voltage drop out, induces crass talk problems and other unwanted side effects*
  - *It also need a lot of interconnections and a lot of power (to be everywhere as fast as possible even if it is not "needed"!)*
  - *Power Dissipation of Bus Structure is poor in energy efficiency because each data transfer is broadcast*
  - *Load capacitance of the entire bus has to be driven during each data transfer*
  - $P = 1/2\ C\ f\ V^2$

- ***=> need of modularity, flexibility and advanced communication protocol between blocks = NoC***

Lifetime considerations

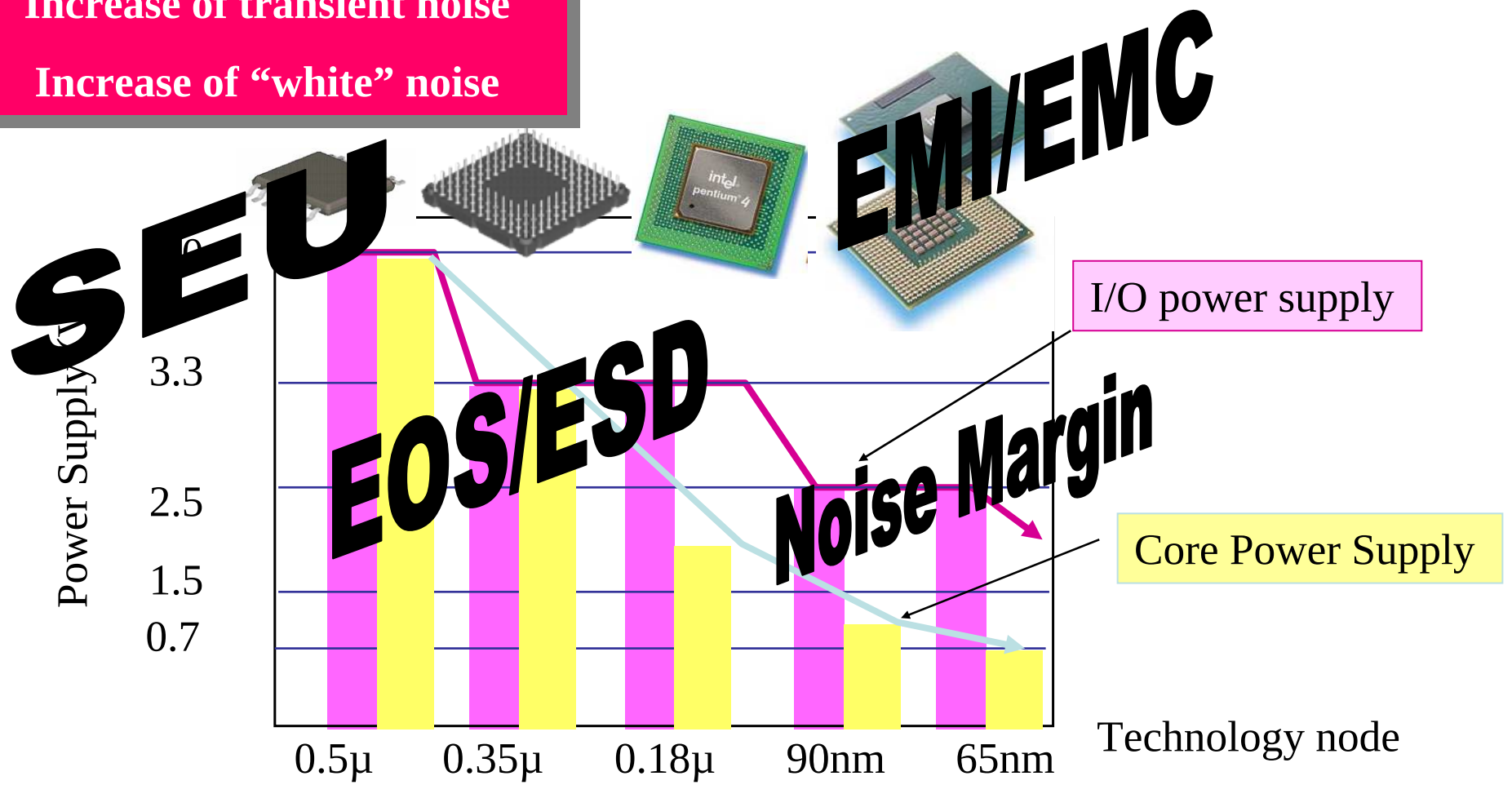
➢ *From Joseph B. Bernstein (University of Maryland/Bar-Ilan University)*



Noise margin issues

Increase of transient noise

Increase of "white" noise



Integration consequences

- ***Direct consequences of integration (reliability Technology Requirements) for a long term reliability targeted between 10 to 100 FITs***
- ***Failure rate per transistor***
  - Overall IC failure rate does not change with time
  - Number of transistors per chip increases
  - Relative failure rate per transistor must decrease
  - Relative from 1 (2005) to 0.2 (2013) => should be divided by 5
- ***Failure rate per m of interconnect***
  - Length of interconnect per chip increases
  - Failure rate per m of interconnect must decrease
  - Relative from 1 (2005) to 0.33 (2013) => should be divided by 3
  - Jmax (A/cm^2) for intermediate wire at 105°C will move from 9 10^5 to 8 10^6
  - Important for reliability is the increase in the number of vias
- ***Reliability issues are manageable (DiR) but are a growing challenge***

NoC intrinsic advantages

➢ *Allow better performances*

➢ *… and a better intrinsic reliability*

- Better internal (local) clock management
  - Low frequency parts
  - =>lower voltage=> lower power dissipation (static and dynamic)
- Less interconnections
  - *power dissipation = temperature / aging)*
  - *Less current = less electromigration, less HCI*

➢ *It can be more*

- Playing with reconfigurability
- Some examples

Lifetime Reliability-Aware Design

- ***two methods for structural redundancy to enhance Lifetime Reliability***
- ***Structural Duplication***
  - Certain redundant microarchitectural structures added to the processor
  - Spare structures can be turned on when the original structure fails, increasing the processor's lifetime
- ***Graceful Performance Degradation (GPD)***
  - Replicated structures that are used for increasing performance for some high parallelism applications
  - Replicated structures are not required for functional correctness so the processor can shut down a failed structure and still maintain functionality, thereby increasing lifetime.
  - Processor with GPD would fail only when all redundant structures of a type fail.
- ***NoC flexibility***
  - Dynamic load allocation
  - Spare the ageed part (slower and higher consumption) when possible
  - Move from HP to LP and vice versa

Conclusion

- ***Nanoelectronic technology allows more and more complex system with an incredible level of performance***
- ***Space is looking for taking advantage of these technologies***

- ***On the other hand long term reliability is challenging***
  - Lifetime, margin, integration issues
  - Managed by DiR … but is getting more challenging

- ***NoC architectures can solve SoC issues***
  - At performance level
  - But also at reliability level

- ***Need to be discussed to prepare the future***